S100 INPUT/OUTPUT BOARD

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0.0 SUMMARY.

This report presents the design, construction & testing of a computer Input Cutput board based on the S100 bus. The board is a versitile I/O card providing a large range of Input/Output combinations port addressed to the computer involved. The project has been designed around the Z80 family support chips. These are used to provide a highly versatile board suited to many applications. This board has been totally designed, laid out, constructed & tested by the author. The basic design considerations are presented in this report and a basic description of how it works is given. Detailed descriptions have not generally been given of the devices used and their timing relationships due to lack of time and space. Detailed manuals are included in the appendicies for this information. Details of basic operation are given along with setting up procedure and onboard port assignments. No information is included on the external devices to be connected as it was considered to be outside the scope of this report. Testing & the problems encountered have been presented although testing was not complete at the time of writing this report.

This report basically sets out to describe the project and its production. The board worked as expected after a number of minor modifications and it is hoped to produce a production run of ten boards in the near future.

INTRODUCTION.

1.1 Background

Over the past few years a large number of development and personal computers have become available. One of the first standardised microcomputer support systems to become available was the Altair which was an 8080 based computer kit which used a 100 pin edge connector to interface it to other computer boards. Signals were defined for each pin of this connector and thus the first major computer bus was born in 1975. A number of the 100 pin connectors were connected in parallel to form the bus system. As later generation computer chips such as the 8085 and Z80 came along, using the same instruction set or an expanded set, more and more systems started to use the bus as the basis of an expandable system. Eventually it was given the name of the 'S100 Bus' and a standard, IEEE696, was formulated to standardise all signals present on the bus to allow greater versatility for the system.

This project is based a-round such a system and is aimed at producing a versatile S100 INPUT/OUTPUT CARD.

1.2 What is it & what does it do?

An Input / Output card is a piece of circuitry which allows the computer to communicate with the outside world through peripheral devices. This board provides both data acquisition and data output links for the computer system. The board is based on a Z80 based system format but should work with any S100 computer system. The board is partially intelligent using Z80 support chips to accomplish the major Input/Output monitoring and functions. These chips have the facility to interupt the processor upon specified conditions

arising allowing the main system processor to continue with other tasks without continually polling the status of particular input or output devices. The board also provides a number of direct nonintelligent ports for later expansion.

Below is a list of the basic data hand-ling facilities provided by this board.

1) 4 softwear are programmable 8 bit parallel ports allowing four possible modes per port. These are:
   - Output (8 bit)
   - Input (8 bit)
   - Bidirectional (8 bit) (2 ports only)
   - Individual Bit controlled input/output.

2) 4 softwear are programmable counter/timer channels allowing direct counting or timing control of external devices. (2 channels wired for softwear are baud rate generation for serial ports.)

3) 2 softwear are programmable serial input/output ports buffered for RS232C operation. Modes available include:
   - Asynchronous data (Byte oriented)
   - Synchronous data (Byte oriented)
   - High-level Synchronous Data Link Control (HDLC) (Bit Oriented)

4) 8 0-5V analog input channels directly port addressed to the CPU & one 7 bit direct TTL input channel.

5) Expansion port decoding allowing provision for a further 15 non intelligent direct access ports located off board. (8 Output ports & 7 Input ports 8 bits wide.)

1.3 Reason for this project.

Having built up a S100 computer system over the last 4 years it was found that to allow adequate expansion of the system for experimentation purposes an increased number of Input/Output (I/C) channels was required. This initial need was first satisfied by piggybacking Z80 PIO chips on the CPU board but it was soon realised that this could not be done as a permanent modification. The next step was to design a prototype card containing two PIO chips and a CTC as well as some bus analysis circuitry. Having completed this board later discussion with other S100 system users revealed a general need for such a card which the hobbyist could build at a reduced price on the normal retail price of these boards (approx $200). Thus this board was then designed including a serial controller chip (SIO) and an ADC. It is Envisaged that this board will be used in the following areas. Control of robotics experiments , enable communication with other computer systems, allowing the connection of remote data collection terminals, printer connection, connection of display devices, Encoding & decoding RTTY transmissions and monitoring & control of a houshold environment.

1.4 Requirements of the system.

This board has been designed to interface directly to any S100 computer system although the most versatile operation will be provided on a Z80 system using mode 2 vectored interupts. The interupt priority daisy chain needs to be hardwired by the user to suit the particular system. The board has been designed to run at 2 MHz but there is no reason why it could not be run at 4 MHz if Z80A chips are used and the ADC clock rate is relinked.

2.0 Design Considerations.

The main design considerations for this project centre a-round the ease with which the board can be interfaced with the computer system and the outside world while maintaining all the standards required to be met by the board.

Board connectors have been used for all external connections and the use of connectors with keying takes account of human error, and prevents insertion of the incorrect plug. The connector layout on the standardised channels has been provided in such a way that direct crimp ribbon cable connection to the plugs and sockets for the cable can be achieved. External connections have been split into groups relating to the type of port. All ports except the serial ports have direct TTL outputs & inputs. Any driver circuitry required for these lines is to be provided off board allowing more space on the board and maximum versitility in the use of the software programmable ports.

TTL devices have been used exclusively for the logic on the board since this is the major type of logic used in microcomputer systems. Low power Schottky devices have been used where possible to reduce the loading and power consumption of the board. A maximum of one Low power Schottky input has been placed on each of the bus pins used. This minimises the total loading on the bus in large systems.

The use of Z80 support chips for the main I/O devices has allowed maximum versatility for the user to apply these devices to whatever application is required. Provision has been made for the use of mode 2 Z80 vectored interupts although the vectored interupts on the bus could be used in conjunction with a programmable interupt controller to provide this function on other types of systems.

An obvious design consideration for this board is the board layout. The S100 specification defines the maximum size board that may be used. The layout had to be designed to provide all the required functions and present them in an orderly fashion to the outside world through connectors along the top of the board. Provision had to be made to allow for a non plated through hole board for the prototype. Thus a reasonable separation distance was required between components on top of the board to allow access to the pads during soldering. The board is to be double sided since such a design could not be achieved using a single sided board. All integrated circuits are provided with sockets except for the voltage regulators. This allows easy replacement if failure occurs or easy retrieval of components should the board be superceeded. When the final board layout is produced the board will be fully plated through. To facilitate prototype testing wirewrap IC sockets have been used and lifted above the board to provide access for soldering. The non plated through prototype also placed limitations on the connector layout since pads could not be connected to pads located on top of the board.

The positioning of the various devices on the board in the computers I/O port map has also required some consideration. A dip switch is provided to locate the 32 locations (20H) occupied by the board to 8 possible positions within the port map. The board may also be removed totally from the port map by the use of a fourth switch.(3 switches used for address). All the user programmable chips have been placed in the first 16 (10H) port locations. The order of these Z80 chips reflects the interupt priority chain order with the CTC reflecting the highest priority followed by the SIO & then the PIOs. This

order reflects the relative interupt duty that would be encountered from such devices. The ADC and expansiom ports have been placed in the second 16 port locations on the board. If the user does not wish to use these facilities then they may be left off the board without affecting the operation of the Z80 chips in the lower 16 locations.

The voltage regulation is carried out on board as required by the S100 standard and has been heatsinked. This is really only required on the +5V regulator since no appreciable current is drawn by the ±12V regulators supplying the RS232C interface. Offboard connections can be made to these supplys which may increase this current. The PIO output connectors have been supplied with unregulated bus voltages since it is envisaged that any offboard equipment using these supplies will have it's own regulator for supplies. No onboard indicators have been included since this board has been designed to be housed inside the computer cabinet out of normal sight.

On the original project proposal a prototyping area was specified. During board layout it was found that the area ~~that was~~ available for this was small and it was decided to decode the remaining 8 ports and allow for prototyping off board. The original specification also described a 20ma current loop as being on board. Due to space considerations this will be provided as an external device to be placed in the serial line. The original project proposal is included in APPENDIX A.

3.0 CIRCUIT DESCRIPTION.

The following is a description of the various blocks contained within the block diagram (figure 1)

The data in & out buffers buffer the data from the S100 input & output data bus into a single bidirectional data bus on board. This is achieved using 74LS241 bidirectional data buffers in a complementary format. These are arranged such that when the board is not supplying data to the CPU they function in the read mode. This allows the intelligent chips on board to follow the CPUs activity and detect return from interupt instructions.

The next section is the control signal generation & buffering section. This block generates the Z80 control signals required by the Z80 chips from the standard S100 signals. The main signals that are generated in this section are;

$$IORQ^* = \overline{((SINP + SOUT) + INTAK)}$$

$$RD^* = \overline{(((POC^*.\overline{INTAK}).PDBIN).PWR^*)}$$

$$\emptyset = \bar{\emptyset} \qquad \text{(clock generation)}$$

$$M1^* = \overline{sM1}.POC^* \qquad \text{(This signal is only used for PICs)}$$

$$DI/\overline{DO} = \overline{((\overline{RD^*} + \overline{BE^*}) + OBINT)} \qquad \text{(Data buffer enable)}$$

Note:- In the above equations an overbar denotes inversion while an asterix denotes an active low signal.

The IORQ* signal (I/O Request) includes the interupt acknowledge signal to allow the Z80 chips to detect an interupt acknowledge. INTAK is also used in the generation of OBINT to enable the interupt vector to be placed on the data bus. POC* & INTAK are included in the read signal generation to provide correct interupt operation and enable the Z80 chips to reset when POC* is applied under master reset or initial system power up.

The next section to be considered is the address decoding section. This section comprises of an 8131 6 bit unified bus comparator and a 74LS139 dual 2 to 4 line decoder. The bus comparator is used to compare the top 3 address lines of the 8 bit port address with values set on the dip switch (DS1). If these bits compare true and the enable switch is on and an I/O access is detected then the Board Enable signal (BE*) is asserted. This signal enables the first of the decoders which determines which block of 8 ports requires access. If a port in the lower 16 port block is to be enabled then the second decoder is enabled to select the correct Z80 chip. The two other outputs of the first decoder enable the ADC & Expansion ports respectively. Buffering of all address lines with more than one load is also carried out in this section.

The Interupt control section deals with the acknowledgement and priority of interupts. This circuitry determines the relative priority of the interupting devices on board using the Z80 Interupt Enable Input/Output (IEI/IEO) signals in a look ahead structure. The look ahead structure is employed to allow ample time for the interupt priority to be determined within the interupt acknowledge and return from interupt cycles. If an on board interupt is detected and the board is the highest priority device in the system then the data input buffers will be enabled to allow the interrupt vector to be passed to the CPU. It must be noted that IEI & IEO are not standard S100 signals and as such need to be linked by the user to the desired location in the computers interupt daisy chain. (refer to CTC manual). These lines have been hard wired to unused bus pins for the prototype but the user may wish to link these signals across the top of the boards in the system or use non defined bus pins numbers 65 & 66. Pads have been provided for this.

The power supply section consists of three voltage regulators of the 78 & 79 series. These regulators are used to regulate the unregulated bus supplies, -16V, +8V, +16V, to -12V, +5V ,+12V respectively. The major supply on this board is the +5V supply. The 12V supplies are only used to supply the RS232 interface. These supplies could also be later linked to offboard equipment through the edge connectors. At present the unregulated supplies are supplied to the PIC output connector to supply off board equipment containing its own regulators. This may be changed on the final board layout to provide linking to either regulated or unregulated supplies which shall also be fused. All regulators have been heatsinked although with present board requirments only the +5V regulator need be. Tantalum capacitors have been used to ensure a constant regulation characteristic and 0.01uF 'bluechip' ceramic capcaitors have been placed around the board to filter out any switching spikes from the supply rails.

The Expansion port decoding block consists of a 74154 4 line to 16 line decoder. This is fed with the three least significant address lines and the read/write signal (RD*) to obtain 16 enable outputs for direct access ports. (8 output & 8 input). The first of the input lines is used to enable a 74LS245 in conjunction with the ADC to obtain the EOC (End of conversion) signal from the ADC. The other 7 bits of this port are supplied to the analog input connector to provide extra ttl inputs for switches. The other 15 enable lines and the on board data bus have been wired to connector CN5 which will be used for connecting the external expansion ports.

The ADC (Analog to Digital Converter) used on this board is the ADC0808 which is an 8 channel multiplexed succesive approximation ADC. The chip is wired to start conversion on detection of a write pulse to the appropriate analog input

specified by the 3 least significant address bits. The write pulse latches these bits and starts the conversion. The end of conversion is signified by a high output on bit Ø of the port discussed in the previous section. If desired the EOC signal could be wired to a vectored interupt line to signal to the CPU that the ADC has finished the conversion. The final value can be read by reading from the ADC after conversion is complete. The clock for the ADC (500KHz) is derived from the 2 MHz clock signal on pin 49 using a 7493. The ADC is capable of running at speeds ranging from 10KHz to 1200KHz. Linking adjacent to the 7493 has been provided to change this speed but this should be adequate for most applications. This clock can also be used as an input to the CTC chip for timing purposes. The ADC clock signal has also been provided on the CTC output connector (pin 10) for use in this capacity.

The operation of the three types of Z80 support chips used on this board is given in detail in the respective manuals included in the bibliography. A brief account of their operation only will be given here. All four devices are essentially wired in parallel with a separate chip enable to each. The PIOs require special consideration for the M1 control signal since this pin is also used to reset the chip when a M1* occurs without a RD* or an ICRQ*. This is necessary due to the 40 pin package limitation. Each of the chips occupies 4 port addresses. The PIOs & SIO split these into channel A & B with each channel assigned a control port and a data port. The CTC is split into 4 separate channels each of which is controlled using write operations to that channel. Data is only read from the CTC ports. Below is a table giving the positions of these channels with respect to address lines A0 and A1.

Table for PIOs & SIO.

A1	A0	Action.
0	0	Channel A Data
0	1	Channel A Control
1	0	Channel B Data
1	1	Channel B Control

Table for CTC.

A1	A0	Action.
0	0	Channel 0
0	1	Channel 1
1	0	Channel 2
1	1	Channel 3

The Pio has two separate ports which may be programmed to be Output, Input or individually bit controlled Input/Cutput. Port A can also be programmed to be bidirectional but port B must be placed in the bit control mode since the handshake signals of port B are used for the bidirectional mode. There are Two handshake signals associated with each port. These are; Strobe and ready. These can be used to signify valid data and can also be used to initiate interupts. The PIO also provides individual bit monitoring in the control mode and can be set to interupt on specified conditions.

The SIO is a versatile serial controller chip which can handle a number of different modes. The main types of operation of this port is envisaged to be in the asynchronous or synchronous Byte mode. The device has a 4 byte receive register to allow for high data rates and a two byte transmit register. It may be programmed to send or receive varying byte sizes from 5 bits to 8 bits inserting 1,1½ or 2 stop bits as required in the asynchronous mode. The Baud rate generation for this chip has been achieved by utilising the first two channels of the CTC chip to provide a softwear programmable Baud rate generator. The RS232C buffering has been achieved by using DS1488 & Ds1489 drivers & receivers. The SIO has a wide range of modem control signals available. These have been connected with maximum flexibility in mind. The SIO bonding option selected for this

project was the SIO/O. This option has the clock inputs to the transmitter & receiver of port B tied together internally. Since operation of the Chip with differing receive & transmit rates is not envisaged these pins were to be tied in any case thus this option was selected to preserve the full compliment of control signals for each port. The Sync Inputs & Wait/Ready outputs have been connected to their buffers but have not been wired to the connector since the pin numbering will vary according to the way in which the user wishes to use these pins. They may be left unconnected with no affect on normal asynch. operation. For further details refer to the SIO Technical Manual.

The CTC is the last major block on the block diagram. The CTC can be programmed as either a counter or a timer. In the timer mode it uses the system clock as it's reference dividing it by a prescale factor of 16 or 256. In the counter mode the external trigger lines are used to trigger the counter. In both modes a Time constant is required by the CTC. The CTC loads this time constant and then downcounts until zero is reached. The counter is then reloaded with the time constant and the zero count output cycled. An interupt can be programmed to occur on each zero count thus allowing it's use as a real time clock or a softwear baud rate generator. The Zero count outputs of channels 0 & 1 are used for SIO baud rate generation although use externally is still possible when the appropriate serial port is not in use. The CTC output connector has also been provided with the ADC clock signal for greater user flexibility. For further information refer to the CTC Technical Manual.

NP84IOB card

Connector pin numbering.

CN 2, 4

Conventional	NP84IOB		Conventional
1	1	26	2
3	2	27	4
5	3	28	6
7	4	29	8
9	5	30	10
11	6	31	12
13	7	32	14
15	8	33	16
17	9	34	18
19	10	35	20
21	11	36	22
23	12	37	24
25	13	38	26
27	14	39	28
29	15	40	30
31	16	41	32
33	17	42	34
35	18	43	36
37	19	44	38
39	20	45	40
41	21	46	42
43	22	47	44
45	23	48	46
47	24	49	48
49	25	50	50

CN 5

Conventional	NP84IOB		Conventional
1	1	14	2
3	2	15	4
5	3	16	6
7	4	17	8
9	5	18	10
11	6	19	12
13	7	20	14
15	8	21	16
17	9	22	18
19	10	23	20
21	11	24	22
23	12	25	24
25	13	26	26

CN 1

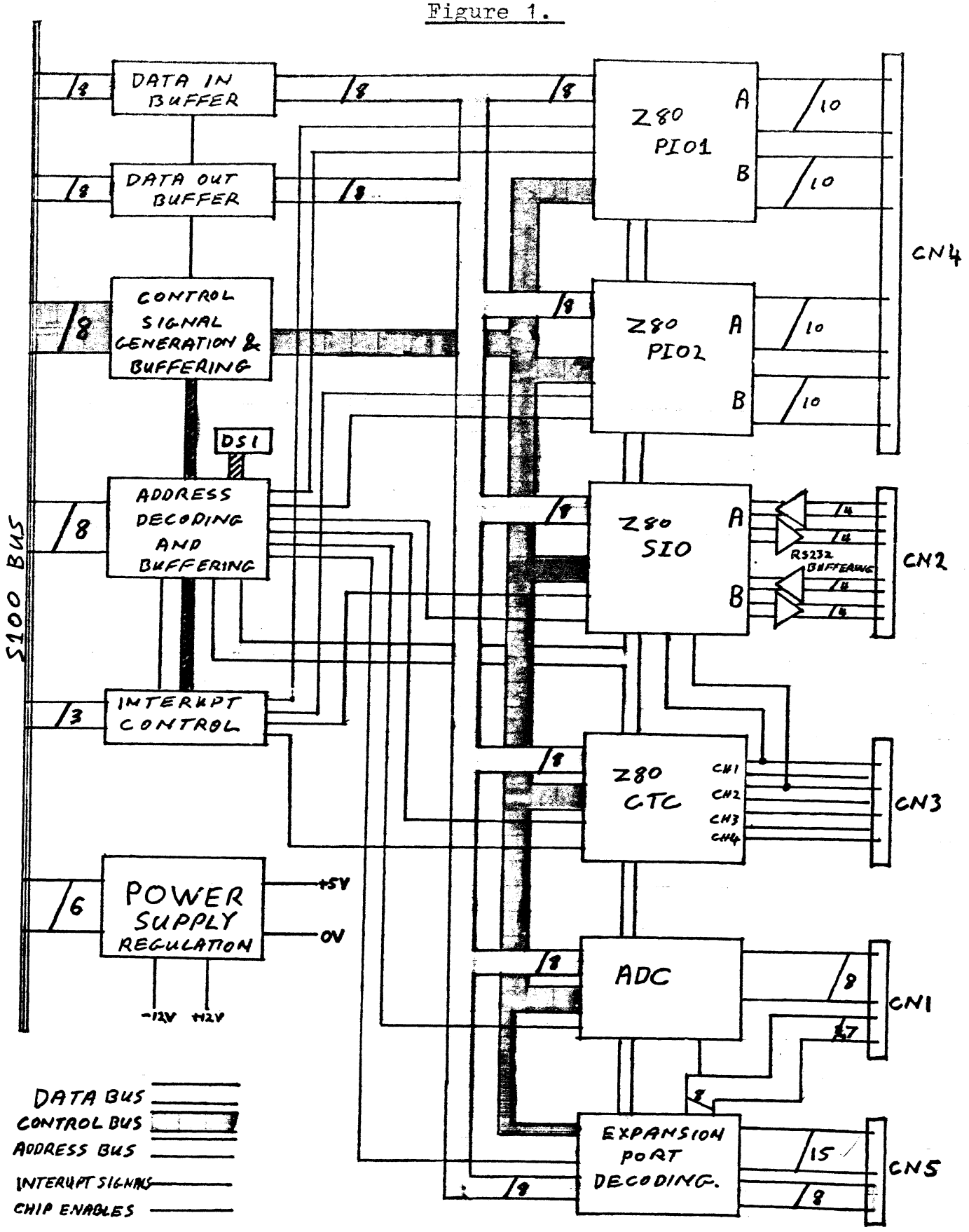
Conventional	NP84IOB		Conventional
1	1	11	2
3	2	12	4
5	3	13	6
7	4	14	8
9	5	15	10
11	6	16	12
13	7	17	14
15	8	18	16
17	9	19	18
19	10	20	20

CN 3

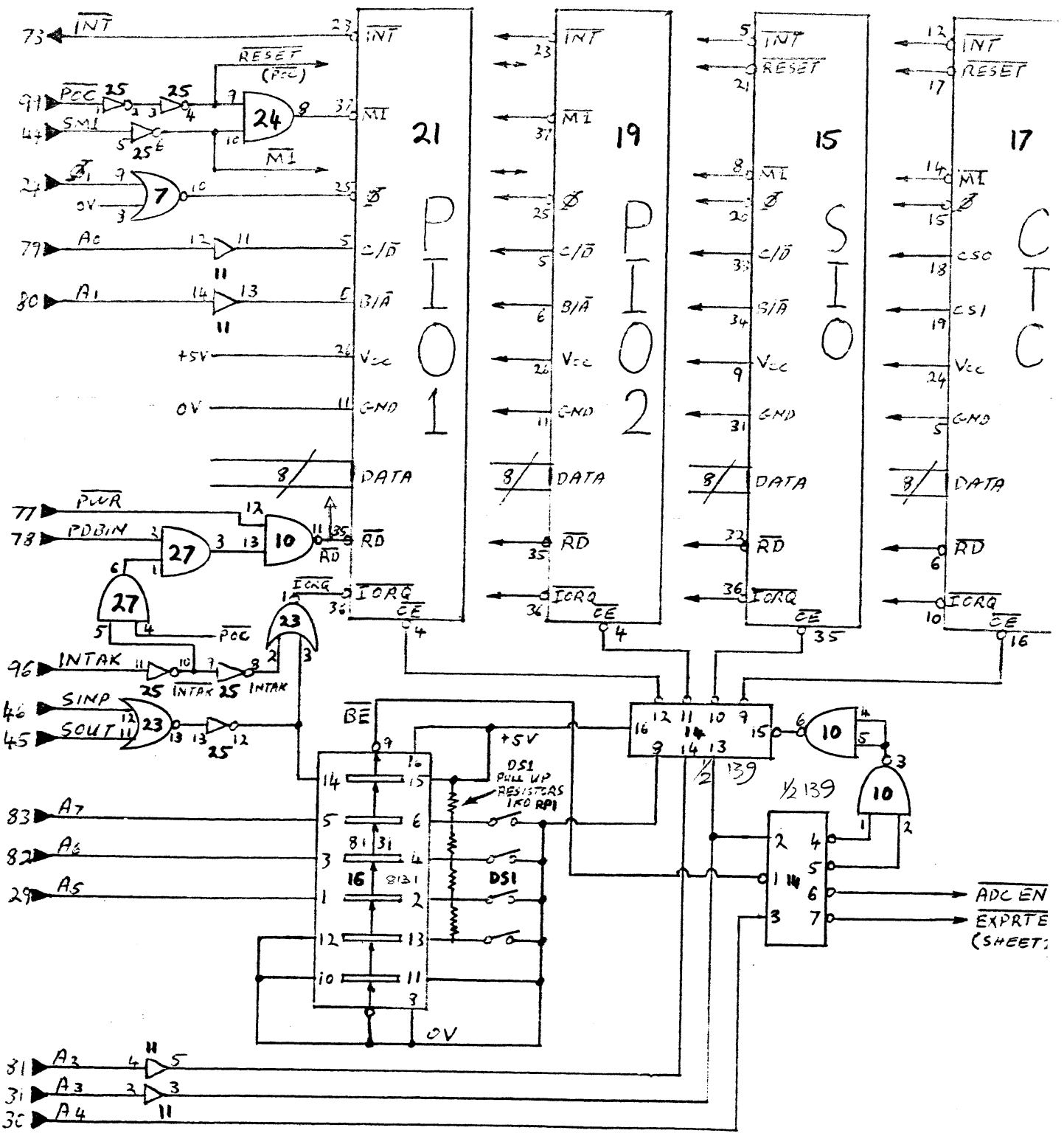
Conventional	NP84IOB		Conventional
1	1	6	2
3	2	7	4
5	3	8	6
7	4	9	8
9	5	10	10

BLOCK DIAGRAM.

Figure 1.



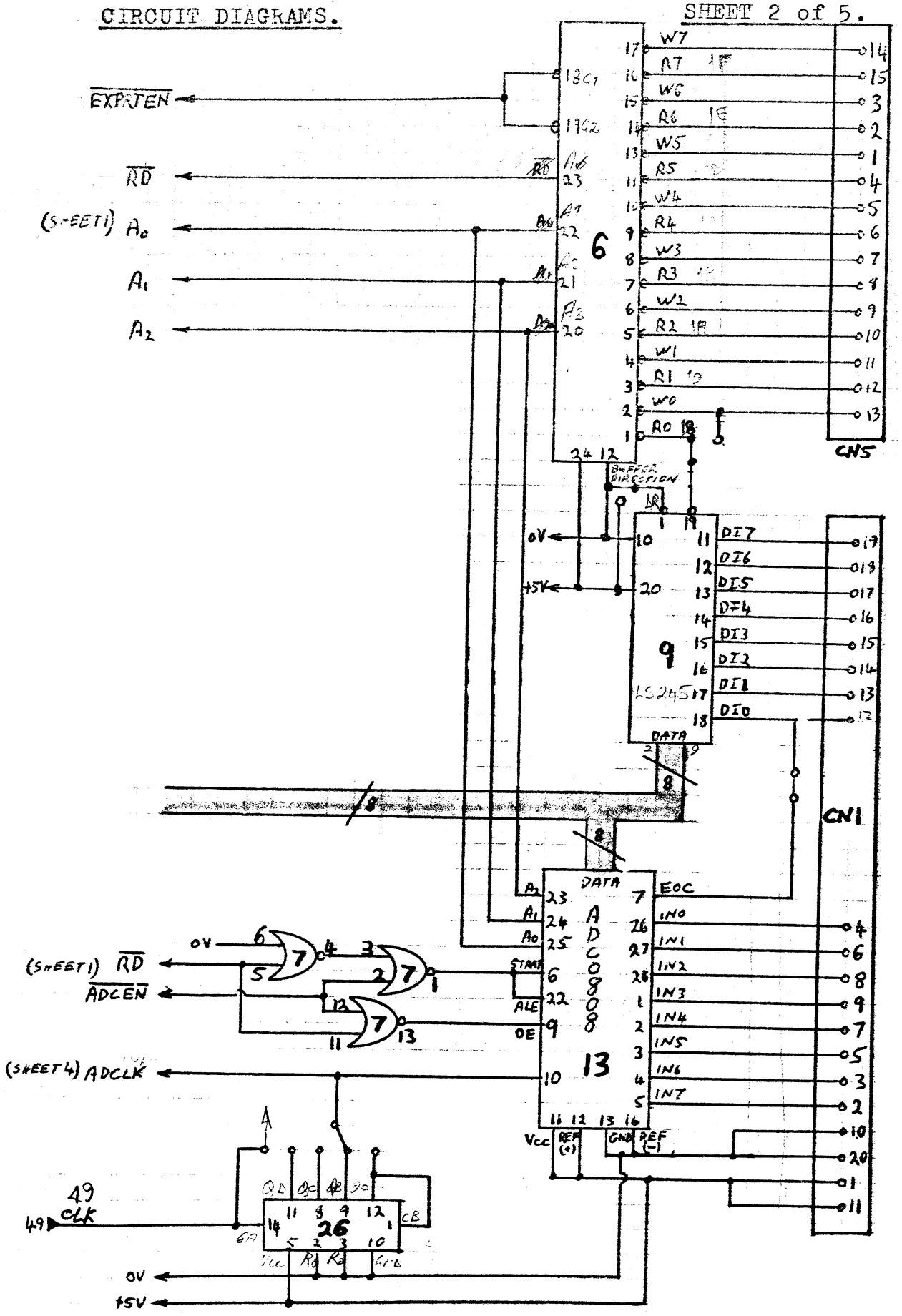
3.1 CIRCUIT DIAGRAMS. SHEET 1 of 5.

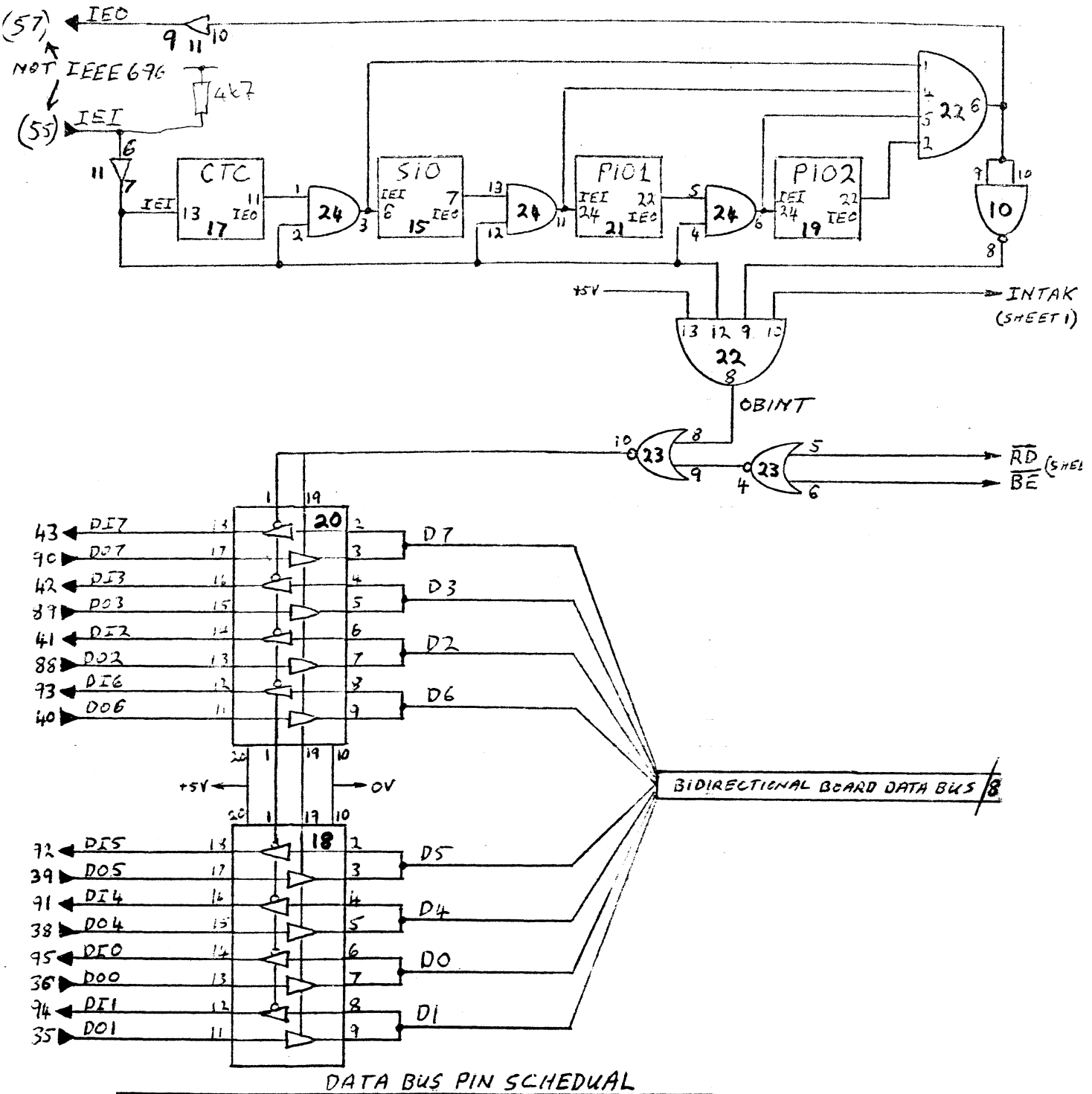


NOTE:- RED NUMBERS INDICATE IDENTIFICATION NUMBERS.

CIRCUIT DIAGRAMS.

SHEET 2 of 5.



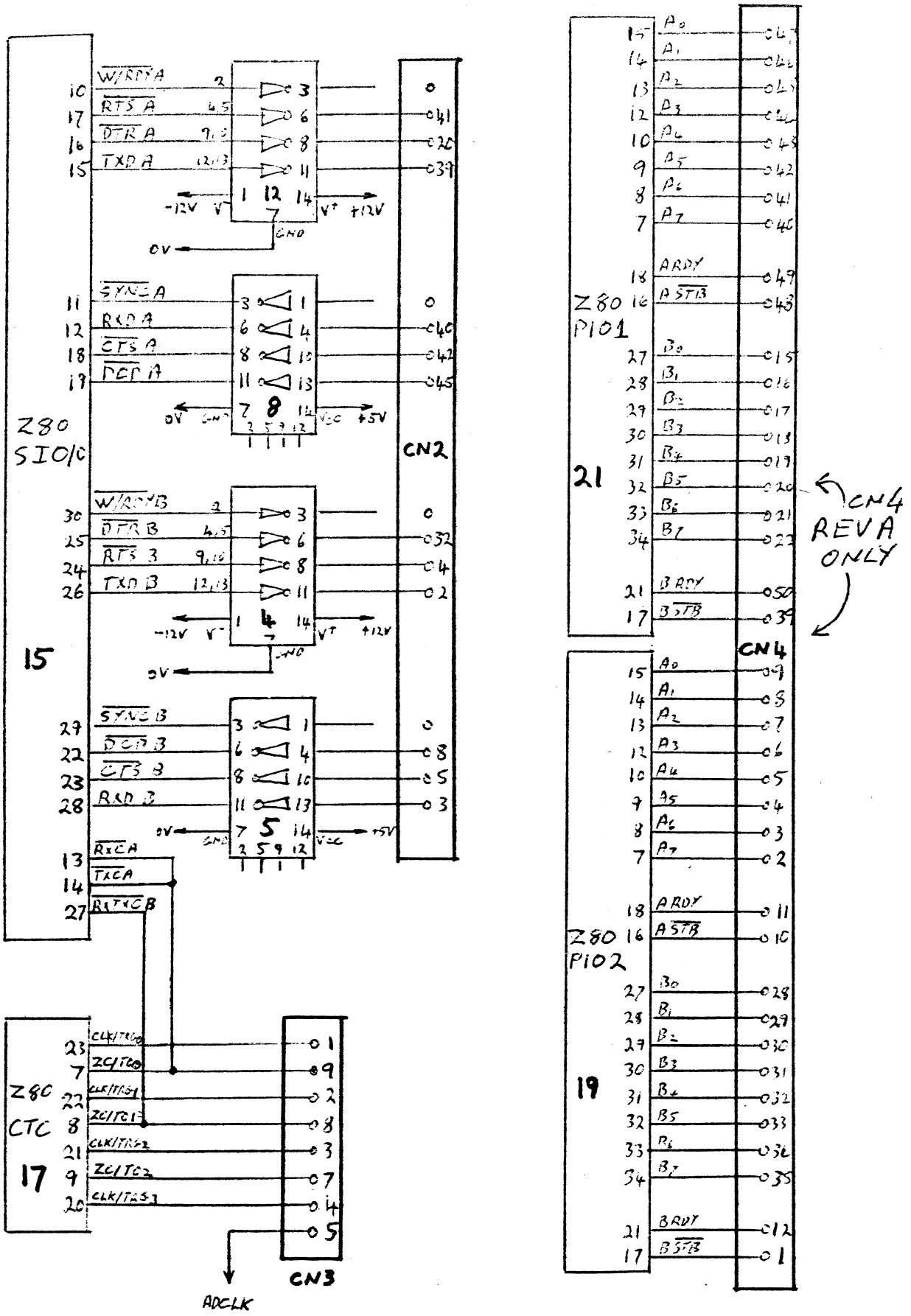


DATA BUS PIN SCHEDUAL

IDENTIFICATION	DESCRIPTION	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
IC18,20	DATA IN BUFFERS	6	8	6	4	4	2	8	2
IC18,20	DATA OUT BUFFERS	7	9	7	5	5	3	9	3
IC19,21	Z80 PIOs	19	20	1	40	39	38	3	2
IC15	Z80 SIO	40	1	39	2	38	3	37	4
IC17	Z80 CTC	25	26	27	28	1	2	3	4
IC13	ADC0808	17	14	15	8	18	17	20	21
IC9	ADC TTL PORT	2	3	4	5	6	7	8	9
CN5	EXPANSION PORT CONNECTOR	26	25	24	23	22	21	20	19
S100	S100 DATA IN	95	94	41	42	91	92	93	43
S100	S100 DATA OUT	36	35	88	89	38	39	40	90

CIRCUIT DIAGRAMS.

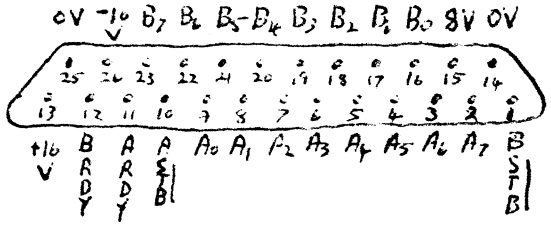
SHEET 4 of 5.

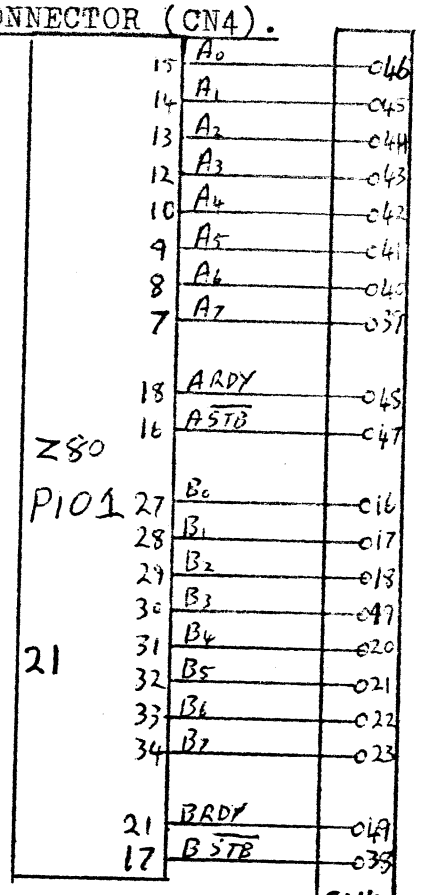


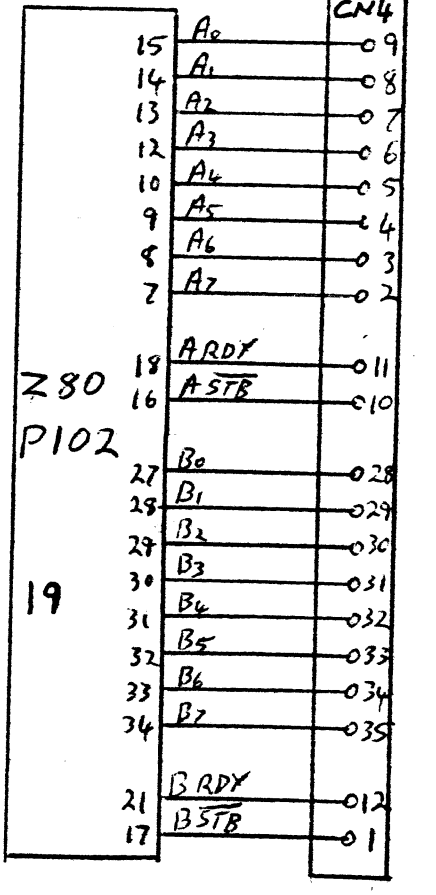
CIRCUIT DIAGRAMS. Revision B. 11-APR-84 SHEET 4a of 5.

REVISION B CIRCUITING OF PIO CONNECTOR (CN4).

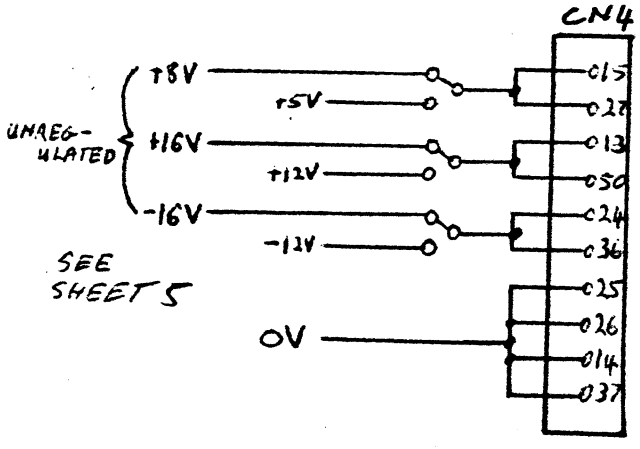
Below is the DB25 layout if a crimp on connector is connected to the header via 50/25 ribbon.





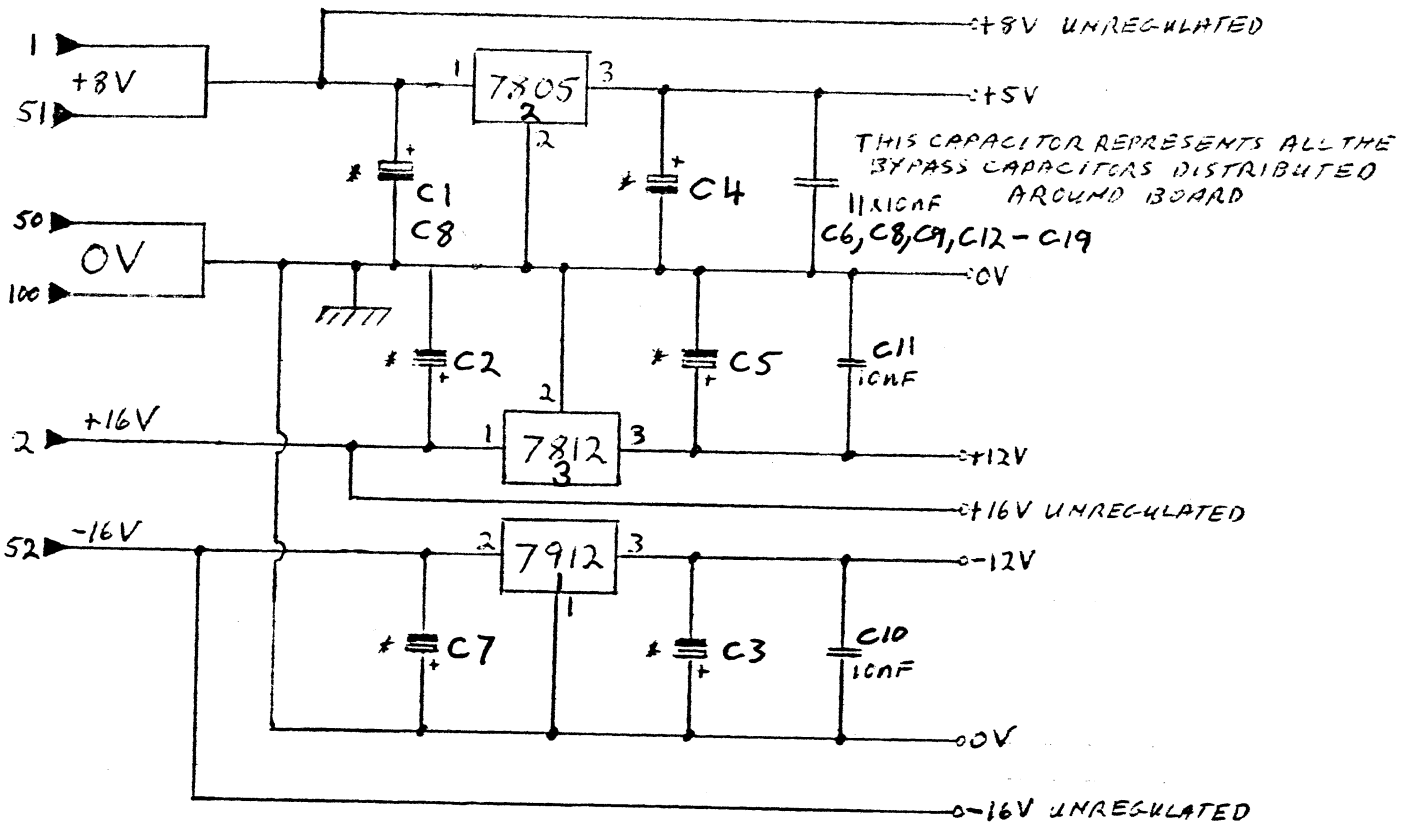


REV B ONLY.

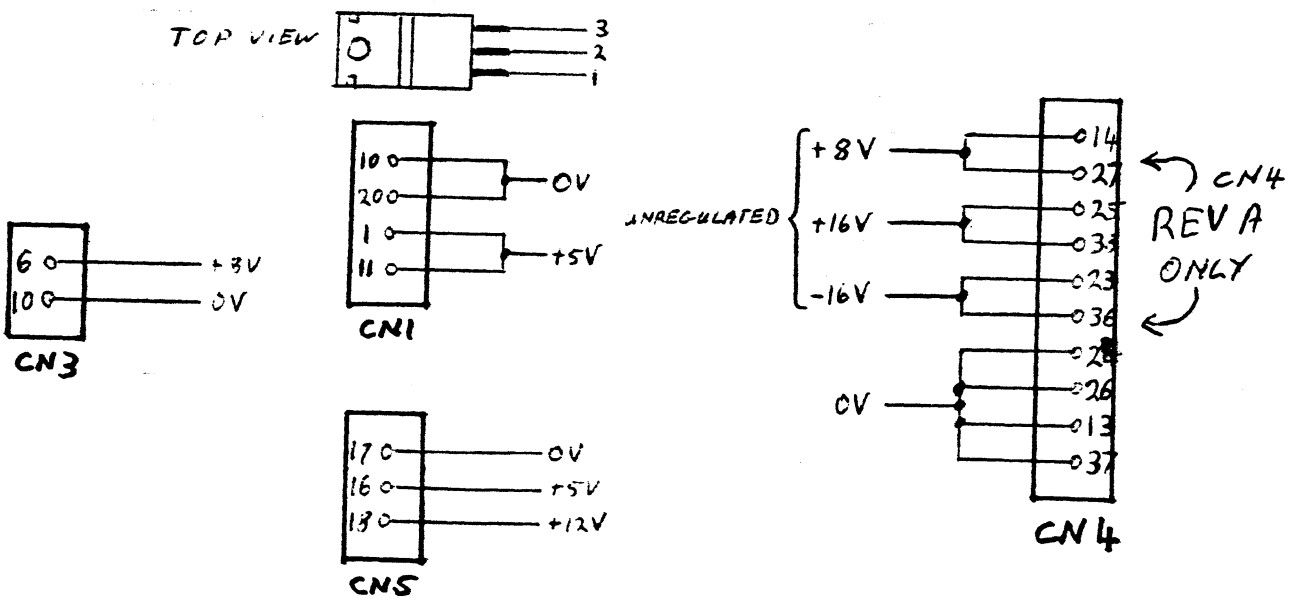


SEE SHEET 5

CIRCUIT DIAGRAMS. SHEET 5 of 5.



* - TANTALUM CAPACITORS.



4.0 CONSTRUCTION.

4.1 The Board.

As mentioned earlier the board is a double sided PCB. The board was laid out double size on Econogrid. Two sheets of econogrid were secured to the layout board with their top edges al-igned. The bottom sheet was taped down while the top sheet could be lifted to provide access for taping on the lower sheet. Most of the tracking on the board was formed using 0.05" tape which reduced to 0.025" tracks. Three crosshairs were used for al-ignment placed in a right triangle at three corners. Since the final board to be produced will be a double sided PLATED through board, the majority of through board connections are made on IC pins. This provided the problem of soldering up the prototype as it is not plated through. Thus adequate spacing was provided between ICs on the board to allow for soldering of raised wire wrap sockets. Generally the proceedure adopted for tracking during the layout was to provide the ac-ross board tracking on the top of the board and to provide tracking from the top of the board to the bottom on the underside. All major connections on the board have been labeled on the underside of the board. Abbreviated IC numbers have also been provided. (ie. 74LS241 = 241). The estimated layout time for this board was 70 hours. The board negatives have been attached to this report in Appendix B. The original layouts are available but their size makes presentation difficult without dammage. Presented on the next pages are the parts list for the board along with the actual component layout. (Figures 2a & 2b)

4.1.1 PARTS LIST. Figure 2a.

Identification	Description.
IC1	7912 1A -12V voltage regulator.
IC2	7805 1.5A 5V voltage regulator.
IC3	7812 1A +12V voltage regulator.
IC4, IC12	DS1488 RS232 driver.
IC5, IC8	DS1489 RS232 receiver.
IC6	74LS154 4 - 16 line decoder.
IC7, IC23	74LS02 Quad 2IP NOR.
IC9	74LS245 Octal bus transceiver.
IC10	74LS00 Quad 2IP NAND.
IC11	74LS367 Hex tristate buffer.
IC13	ADC0808 8 bit 8 channel multiplexed A/D converter
IC14	74LS139 Dual 2 - 4 line decoder.
IC15	Z80 SIO/O Serial Input/Output Controller.
IC16	DM8131 6 bit unified bus comparator.
IC17	Z80 CTC 4 channel counter/timer circuit.
IC18, IC20	74LS241 Octal buffer/line driver.
IC19, IC21	Z80 PIO Parallel Input/Output Controller.
IC22	74LS21 Dual 4IP AND.
IC24, IC27	74LS08 Quad 2IP AND.
IC25	74LS04 Hex inverter.
IC26	74LS93 Divide by 16 counter.
RP1	4 * 1KO resistor pack. (5 pin SIL)
DS1	4 pole dip switch (8 pin DIL)
CN1	20 pin RT angle board connector (single key)
CN2	50 pin RT angle board connector (double key) (with ejectors)
CN3	10 pin RT angle board connector (Single key)
CN4	50 pin RT angle board connector (single key) (with ejectors)
CN5	26 pin direct board connector (single key)

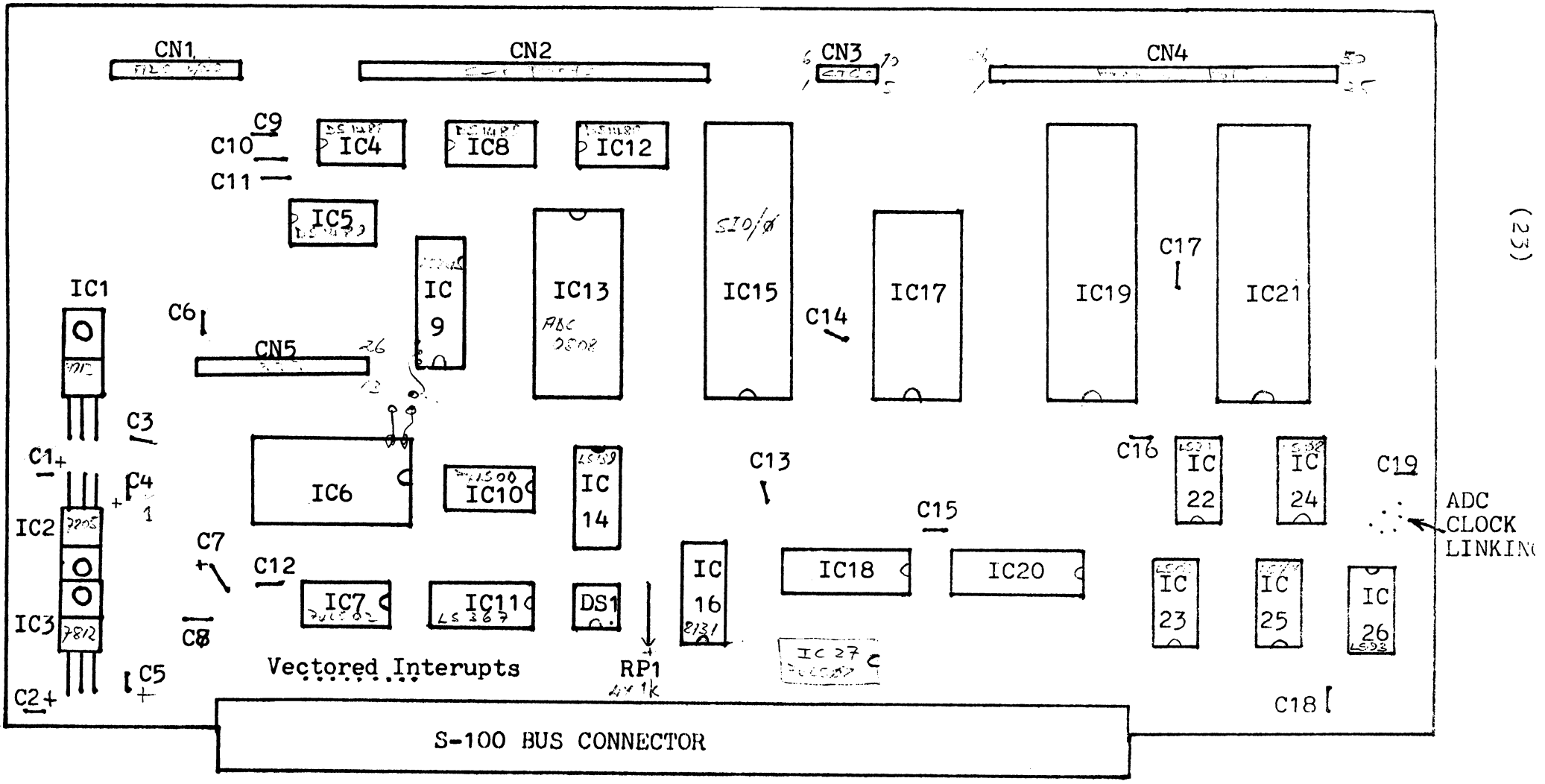
Note:- All connectors without ejectors unless

PARTS LIST (cont.)

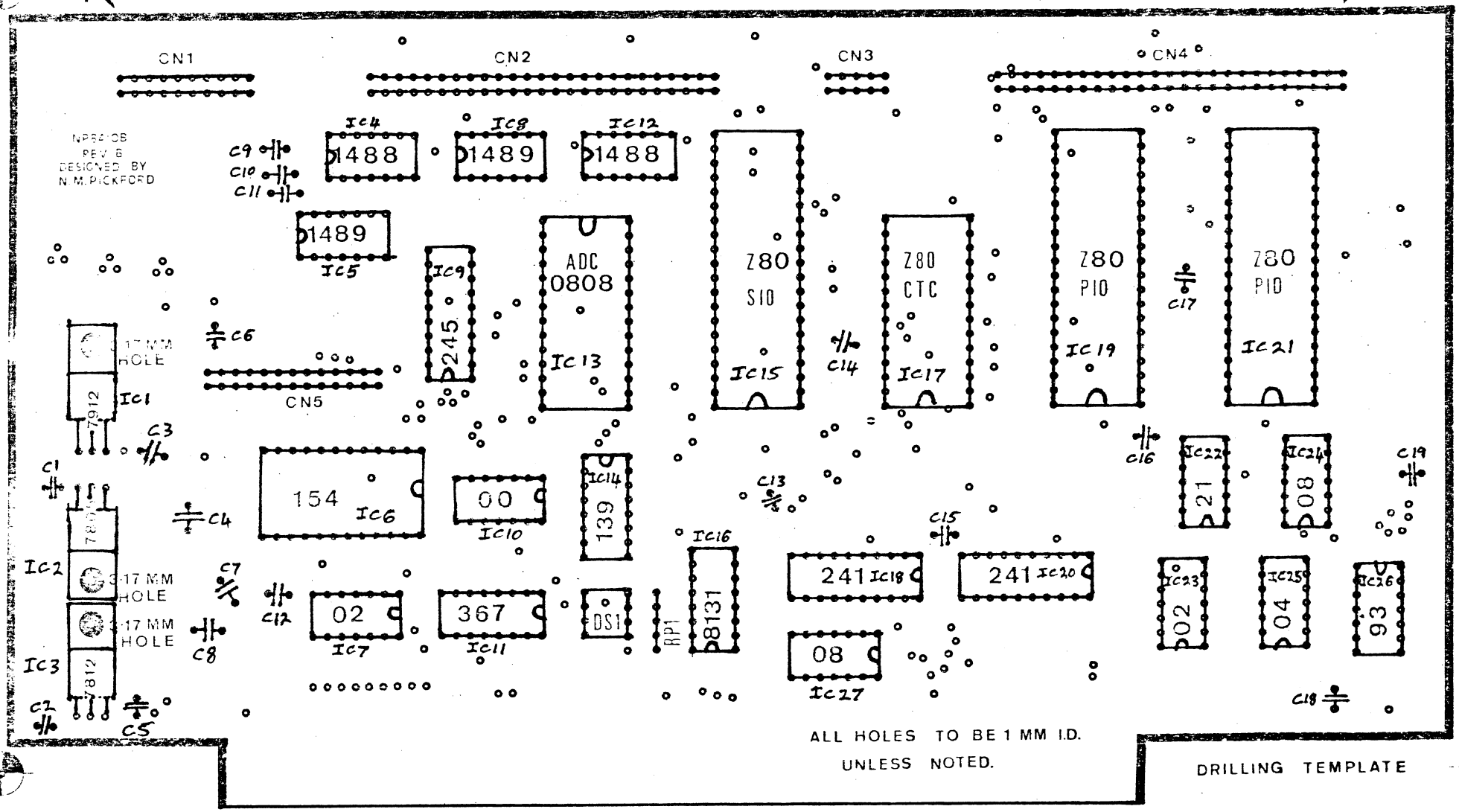
Identification	Description.
C1	47uF 16V Tag Tantalum capacitor.
C2,C7	47uF 25V Tag Tantalum capacitors.
C3,C5	4.7uF 16V Tag Tantalum capacitors.
C4	4.7uF 16V Tag Tantalum capacitor.
C6,C8-C19	0.01uF 'bluechip' ceramic bypass capacitors.
HS1-HS3	TO-220 heatsinks
MISCELLANEOUS	3 * 1/8" X ½" bolt & nuts.
	Heatsink compound.
	3 * 40 pin IC sockets
	2 * 28 pin IC sockets
	1 * 24 pin IC socket
	3 * 20 pin IC sockets
	3 * 16 pin IC sockets
	12 * 14 pin IC sockets
	Double sided PCB (NP8301)
	Wire wrap wire for hardwired connections.
	50g of 0.71 solder.

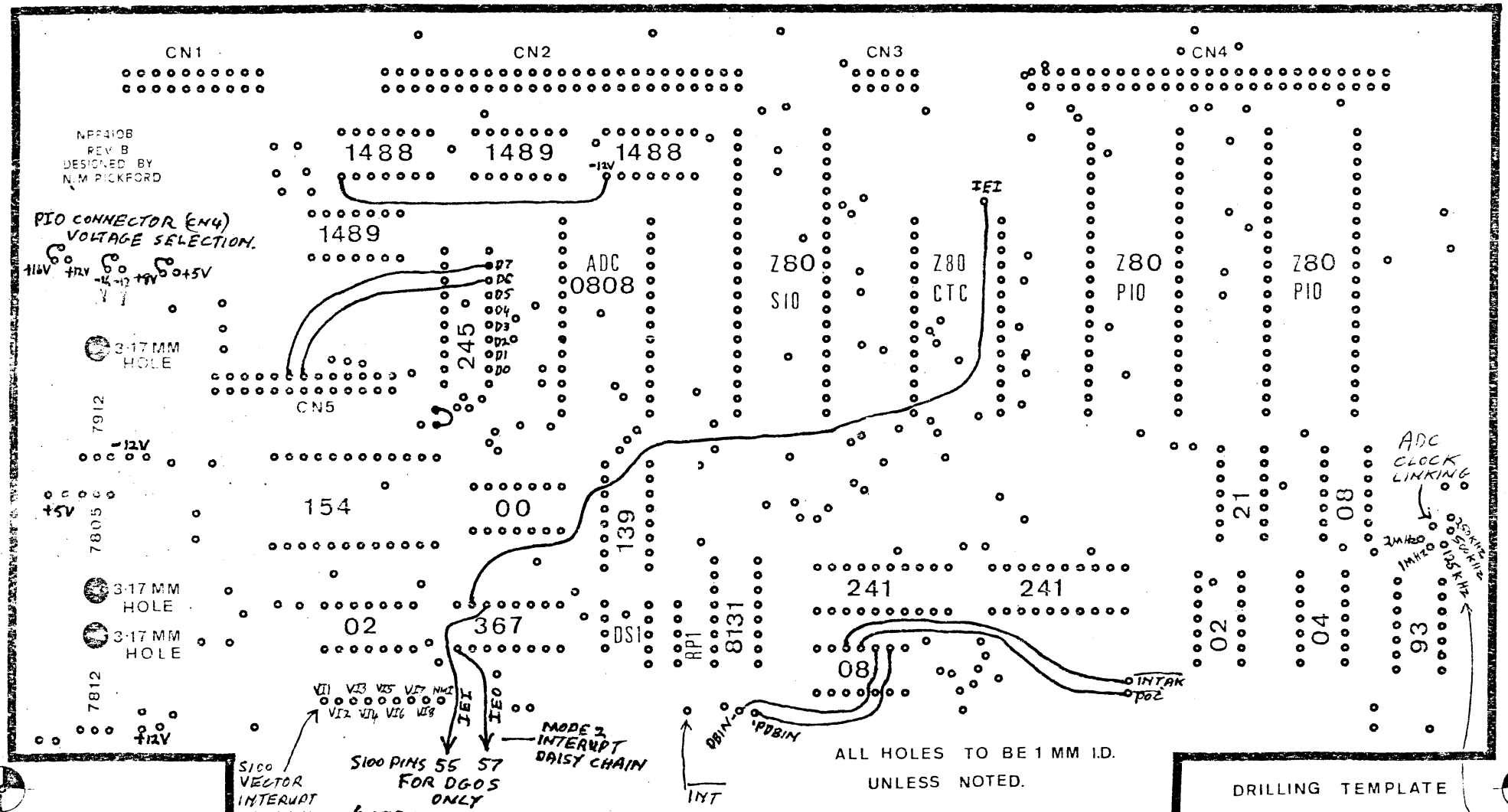
PRINTED CIRCUIT BOARD LAYOUT. REV A

Figure 2b.



REDUCE TO 9 INCHES





ON BOARD LINKING REQUIRED

INTERUPT LINKING PIN DESIGNATIONS

NOTE:- device part numbers have been shortened.

ie 74LS367 ≡ 367

DS1489 ≡ 1489

DM8131 ≡ 8131

frequencies quo
are for a 2MHz
clock signal on
pin 49 of S100 bu

4.2 Construction of the Board.

The board was submitted for etching on 29/SEP/83 and recieved on the 7/OCT/83. The board was first drilled and then enquiries made about tin plating the main connector. It was found that there was no solution available and thus the main S100 connector has not been plated YET. Construction began with the insertion of all board feed through links. The IC sockets were inserted next, raising them approximately 1 cm above the board to allow soldering access. The largest ICs sockets were inserted first. The order of insertion also depended on the ease of access due to IC sockets al-ready inserted. After all sockets were installed the output connectors were added along with the voltage regulators & associated hardwear. All capacitors were then inserted along with the resistor pack & dip switch which were directly soldered in. The initial powerup was the applied to the board to check all supply voltages and IC supply rails. After this check ALL ICs were inserted into their respective sockets and the board reinstalled in the computer for the initial tryout & testing.

4.3 Setting Up.

The dip switch (DS1) was set up to the port address required for testing and the board enabled. The set up details for this switch are presented on the following page. The hardwired links were installed next to configure the interupt daisy chain, Supply data lines D6 & D7 to the Expansion port connector (Multiparallel ports), supply -12V to IC12. The board was then inserted, a system reset applied, & test programs run.

4.3.1 DIP SWITCH SETTING.

Below is a table giving the position of the board in the computers I/O port map in relation to the DIP switch settings. (DS1).

S4	S3	S2	S1	Board position.
0	0	0	0	00H to 1FH
0	0	0	1	20H to 3FH
0	0	1	0	40H to 5FH
0	0	1	1	60H to 7FH
0	1	0	0	80H to 9FH
0	1	0	1	A0H to BFH
0	1	1	0	C0H to DFH
0	1	1	1	E0H to FFH
1	X	X	X	Board disabled. ←

0 = Switch in On position.

1 = Switch in Off position.

S4 is closest to the top of the board.

4.4 Operation.

Once the initial system set up proce-dures have been completed operations using the board may commence. Note; When setting up the boards position in the computers port map ensure that no conflict of addressing will occur with other devices located in the same area. This may cause the destruction of the Data input buffers on this board or the conflicting device. The port layout of this board is presented in figure 3 on the next page. The board can be accessed using the normal Input & Cutput operations of the CPU. The programmable chips in locations OOH to OFH will need to be set up in the desired mode before use of these devices can be made. The information pertaining to the set up proceedures can be found in the Technical manuals attached in Appendix C.

The operation of the A/D converter is as outlined below.

(a) Write anything to the port address corresponding to the desired ADC input channel. This will select the channel and start the conversion.

(b) Read port 18H until bit 0 becomes set. This signals the end of the conversion.

(c) The converted data may now be read from the original ADC channel

For further information on the ADC see reference 5

The Expansion ports operate like any direct access parallel ports. The exact operating proceedure will depend on the type of device connected to the Multiparallel port connector. (ie. Latched or Unlatched Cutputs).

4.4.1 On Board I/O Port Addresses.

Below is a table of the port addresses assigned on the board. The locations quoted should be added to the base board address set up using DS1

00H	PORT A DATA	Z80 PIO No.1
01H	PORT A CONTROL	
02H	PORT B DATA	
03H	PORT B CONTROL	
04H	PORT A DATA	Z80 PIO No.2
05H	PORT A CONTROL	
06H	PORT B DATA	
07H	PORT B CONTROL	
08H	PORT A DATA	Z80 SIO/0
09H	PORT A CONTROL	
0AH	PORT B DATA	
0BH	PORT B CONTROL	
0CH	CHANNEL 0	Z80 CTC
0DH	CHANNEL 1	
0EH	CHANNEL 2	
0FH	CHANNEL 3	
10H to 17H	A/D CONVERTER PORTS. Write = Start conversion on respective input. Read = Converted value from previous conversion.	
18H	Read only. ADC End of conversion signal, bit 0. Other 7 bits TTL inputs from ADC connector.	
18H	Write only.	
19H to 1FH	Expansion port positions (7 read ports, 8 write ports).	

5.0 TESTING.

Testing of the board involves installing the board in the computer system and using programs & external test devices to determine the operation of the board. This testing involves systematically testing all the functions on the board starting with the simple basic functions and working through to the more complex functions such as interupt servicing. It is very difficult to formulate one test program to carry out all these functions in the short ammount of time allocated for the project.

Testing began with the initial chip checkout, checking for incorrect insertion and voltages. The CPU was then started with the the board in place and checked for normal operation. Having asertained that the board does not interfere with normal operation the basic read & write operations to the board were tested. A subroutine was formulated to display the value of all system ports on the screen at any time. Using this it was possible to observe the effects of the read status of different ports and gain a direct indication of the ports response.

The first test programs run attempted to program the Z80 support chips and check their operation in the basic modes. The major demonstration test was to connect the parallel printer to the PIO ports and program it for correct operation. The operation of the ADC was next checked and found to be correct except for the end of conversion signal. After modifications to the TTL input buffer associated with the ADC this operation checked out successfully. Output operation of the RS232 ports was next checked using signal detection equipment although a direct connection to another serial device was not achieved.

The next main feature requiring testing was the interupts. It was found that these were not working correctly in the Mode 2 interupt mode. Further investigation revealed that the board

was not responding to a master reset and clearing all the Z80 chips as required. This was finally tracked down to be a logic error in the generation of the read signal (RD*). After the appropriate modifications had been carried out the interupt structure of the system was tested and found to work as expected. The interupt daisy chain has been checked for correct operation logic wise although extensive testing will be required to determine any flaws under multiple interupt situations.

5.1 PROBLEMS.

A number of small problems were revealed during the testing of this board and they have been detailed below. Wherever possible modifications have been made and included in the circuits of this report.

1) On initial tryout the Z80 chips could not be accessed in the proper manner. It was found that a top of board IC pad had missed out on soldering. This problem was rectified by soldering the joint. (IC25 pin 5)

2) it was found that spurious data was entering the data bus 0 line on the board. This was traced to an incorrectly inserted bypass capacitor between the ADC end of conversion signal and the internal data bus 0 line. This was corrected by removing the capacitor. This problem occured due to the lack of an accurate layout of where all capacitors were to reside. This has since been rectified.

3) It was found that the End of conversion signal from the ADC was not reaching the data bus. This was traced to incorrect pin allocation to the buffers in IC 9 which was a 74LS541 at that time. The buffers had been reversed during layout. This problem was solved by replaceing the 541 with a 74LS245 which is a bidirectional bus transceiver with an equivilent pin out.

The onboard track between pins 19 & 1 of IC 9 ~~were~~ was cut and pin 1 straped to ground to program the correct direction. Pin 19 was used as the enable as previously circuited. After the completion of this modification the buffer and ADC EOC signal worked as expected. This modification will be incorporated on the final board with linking on the direction enable and chip enable to allow the user to relink this port to be an output port if the ECC signal can be provided through other means such as interupts.

4) It was found that the interupt acknowledge cycle for the Z80 chips was not being completed and thus causing the system to crash. It was also found that the PIOs were not resetting on a master system reset. The PIOs use a combination of the M1*, IORQ* & RD* signals to indicate a reset and thus these were suspected. It was found that RD* was becoming active during the incorrect part of the reset cycle and that the same fault was occuring during an interupt acknowledge cycle. This problem was due to incorrect decoding of the RD* signal from the S100 bus. Originally RD* was formed by NANDing the PWR* and PDBIN signals. The modification involved ANDing INTAK* and POC* together and then ANDing the result with PDBIN to obtain the original PDBIN input to the NAND gate. This modification required interupting the PDBIN line only and this was accomplished by removing a board feed through link. IC27 was subsequently added to the back of the board to provide the extra two AND gates required by the modification since no spare gates were available on the board. After the completion of this modification the interupt acknowledge and reset cycles were found to operate normally.

5) During the testing of the CTC it was found that the address lines CS0 & CS1 had been interchanged during the board layout.

This swap in address lines causes port 1 to appear in port 2s position and vise versa. This problem has not been rectified as yet but will be fixed during the relayout of this board.

6) During the layout phase the PIO connector CN4 was laid out reverse to that intended. This change in layout ment that the envisaged ribbon cable connection is not realisable. Thus sockets at the end of the connector ribbon have been individually pin soldered to obtain the required signal layout on the sockets. This again will be modified at the time of the relayout for production of a plated through board.

7) During Assembly it was noticed that the +12V & +5V regulators had been placed too close together, not providing enough room for a normal nut to fit on each securing bolt. The solution to this problem was to file one side of each of the nuts. This solution had the bonus of locking the two nuts together allowing easy tightening of the screws. This layout will be rectified in the second layout.

8) During construction & testing it was noticed that it may be necessary to fuse the unregulated connector voltage lines on the board since they are not current limited. Also provision will be made in the future for linking of these lines to either regulated or unregulated lines as the user requires.

9) Finally the only other significant problem encountered is the non plated S100 edge connector. Oxidisation on this connector could cause poor board performance & reliability and thus this will be plated when the plating equipment is available.

5.2 SOFTWEAR TEST PROGRAMS.

Dissasemblies of some of the test programs used during the testing of this board have been included in Appendix D.

6.0 CONCLUSION.

This project has produced a board which is very versatile in being able to provide a wide range of general I/O facilities. The board has been designed to work with any S100 system and as such would provide the average user with ample interface channels to the outside world. The use of the Z80 support chips on this board increases it's versatility owing to their programmable nature. More importantly a board has been produced which will allow the user in the hobbyist category build a versatile interface with most of the required features for a reasonable cost.

The educational aspects of this project have been far reaching. Much has been learned about interface techniques and the design of complex boards. A solid introduction to double sided board techniques has been achieved along with experience in debugging hardwear with limited equipment. The operation of the various devices used on this board has become very well known and little difficulty is had in understanding their operation having interfaced and tested them. The serial device is the main device yet to be completely fathomed but this is mainly due to not being able (as yet) to test it in it's various serial modes.

It is hoped to produce a run of ten of these boards in the future to sell to hobbyist/builders who have been waiting for such a board to be produced. A second relayout of the original layout will be completed along with a drilling mask to allow a PCB manufacturer to produce a plated through, solder masked double sided board with a gold plated edge connector. The envisaged price of this board is $55. A manual comprising part of this report will also be produced to aid the construction & use of this board.

7.0 BIBLIOGRAPHY.

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2) Zilog Inc., ZILOG 1982/83 Data Book, U.S.A. 1982.

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5) National Semiconductor, 1981 CMOS DATABOOK, Victoria, Dominion Press, 1981.

6) Zilog Inc., Z80 SIO TECHNICAL MANUAL, U.S.A. 1978.

7) Zilog Inc., Z80 PIO TECHNICAL MANUAL, U.S.A. 1978.

8) Zilog Inc., Z80 CTC TECHNICAL MANUAL, U.S.A. 1978.

9) Zilog Inc., Z80 Assembly Language Programming Manual, U.S.A. 1980.

10) Bursky, Dave. The S-100 BUS Handbook. U.S.A. HAYDEN BOOK COMPANY, 1980.

APPENDIX D

TEST PROGRAMS.

This appendix contains disassemblies of the major programs used in the testing of the board. These machine code subroutines were combined with high level programs in BASIC to provide an easier testing enviroment.

BELOW IS A BASIC PROGRAM USED DURING TESTING

```
10 P=64:! SET UP BOARD POSITION.
20 !
30 REM *SET UP PORT DISPLAY ROUTINE *
40 I=16RDB00
50 READ D%:IF D%<0 THEN 70
60 POKE(I)=D%:I=I+1:GOTO 50
70 DATA 33,0,243,77,237,120,119,44,194,3,219,201,0,0,0,0,205,0,219,195,16,219,-1
80 DEF FAA=16RDB00:! DEFINE MACHINE CODE PORT DISPLAY FUNCTION.
90 !
100 ! *NOW TO SELECT OPTIONS *
110 PRINT"OPTIONS ARE:-"
120 PRINT"T - PROGRAM CTC FOR 'TIMES SQUARE DISPLAY' OPERATION."
130 PRINT"P - PRINT OUT DECIMAL PORT VALUES (PORTS 64-95)"
140 PRINT"C - PROGRAM ANY PORT WITH DECIMAL DATA."
150 PRINT"J - DISPLAY DECIMAL VALUES FOR ANALOG INPUTS 2 & 3"
160 PRINT"A - OBSERVE ANY ADC CHANNEL INPUT"
170 INPUT"FUNCTION";A$:IF A$="A" THEN 410
180 IF A$="P" THEN 500
190 IF A$="C" THEN 320
200 IF A$="J" THEN 540
210 D=8:! TIMER TIME CONSTANT.
220 OUT(P+12)=2R00000101:!PROGRAM CTC CHANNEL 0 TO BE A TIMER
230 OUT(P+12)=D
240 L=57:! LENGTH OF DISPLAY
250 OUT(P+13)=2R01000101:!PROGRAM CTC CHANNEL 1 TO BE A COUNTER.
260 OUT(P+13)=L
270 OUT(P+5)=15:!PROGRAM PIO2 CHANNEL A TO BE AN OUTPUT PORT
280 INPUT"DATA TO DISPLAY";D%:OUT(P+4)=D%:!SEND DATA TO DISPLAY.
290 K=FAA:GOTO 280:!DISPLAY PORT MAP AND LOOP.
300 !
310 !PROGRAM PORTS WITH DECIMAL DATA.
320 PRINT CHAR$(12):!CLEAR SCREEN.
330 INPUT"PORT";Q%:IF Q%<0 OR Q%>255 THEN 110
340 INPUT"DATA";O
350 IF O<0 THEN PRINTCHAR$(11);CHAR$(11);:GOTO 330
360 OUT(P+Q%)=O:!OUTPUT DATA TO SELECTED PORT.
370 PRINT IN(P+Q%);:!READ & PRINT DATA FROM PORT.
380 PRINT CHAR$(11);
390 K=FAA:GOTO 340:!PRINT OUT PORT MAP & LOOP
400 !
410 !OBSEVATION OF ADC CHANNELS.
420 INPUT"WHICH ADC CHANNEL (0-7)";C%
430 IF C%<0 OT C%>7 THEN 410
440 OUT(P+C%+16)=0:!START ADC CONVERSION BY WRITING TO CHANNEL..
450 K=FAA:!PRINT PORT MAP
460 K%=IN(P+24):IF K%/2=K%\2 THEN 440:!IF CONVERSION COMPLETE THEN START NEXT ON
E.
470 GOTO 450
480 !
490 !PRINT OUT PORTS 64-95
500 FOR I=64 TO 95:PRINT IN(I);:NEXTI
510 PRINT CHAR$(13);CHAR$(11);CHAR$(11);:GOTO 500
520 !
530 !PRINT OUT VALUES FOR ADC INPUTS 2 & 3
540 PRINT CHAR$(12)
550 OUT(P+18)=0:PRINT IN(P+18);
560 K=FAA
570 OUT(P+19)=0:PRINT IN(P+19)
580 K=FAA
590 PRINT CHAR$(11);
600 K=FAA
```

```
DB00:  21 00 F3      LD   HL,F300  SET TO BOTTOM 1/4 of screen
DB03:  4D            LD   C,L
DB04:  ED 78         IN   A,(C)        PORT-SCREEN
DB06:  77            LD   (HL),A
DB07:  2C            INC  L                DISPLAY ROUTINE
DB08:  C2 03 DB      JP   NZ,DB03
DB0B:  C9            RET

DB0C:  00            NOP
DB0D:  00            NOP
DB0E:  00            NOP
DB0F:  00            NOP
DB10:  CD 00 DB      CALL DB00      CONTINUOUS PORT DISPLAY ROUTINE
DB13:  C3 10 DB      JP   DB10

DB16:  00            NOP
DB17:  00            NOP
DB18:  00            NOP
DB19:  00            NOP
DB1A:  00            NOP
DB1B:  00            NOP
DB1C:  00            NOP
DB1D:  00            NOP
DB1E:  00            NOP
DB1F:  00            NOP
DB20:  CD 00 DB      CALL DB00
DB23:  FB            EI          INTERUPT SERVICE ROUTINE
DB24:  ED 4D         RETI
DB26:  00            NOP
DB27:  00            NOP
DB28:  00            NOP
```

SIO TEST PROGRAM.

```
                00264 ;PROGRAM TO SET UP A 110 BAUD SERIAL PORT USING THE SIO.
DC00            00265          ORG     0DC00H
DC00 3E05       00266          LD      A,05H    ;INITIALISE CTC &
DC02 D34C       00267          OUT     (4CH),A  ;SET PRESCALER = 16
DC04 3E2F       00268          LD      A,47     ;LOAD CTC TIME CONSTANT
DC06 D34C       00269          OUT     (4CH),A
                00270 ;NOW TO SET UP SIO...
DC08 3E03       00271          LD      A,03H    ;SELECT WR3
DC0A D349       00272          OUT     (49H),A  ;
DC0C 3E41       00273          LD      A,41H    ;PROGRAM RECIEVE 7 BITS/CHAR
DC0E D349       00274          OUT     (49H),A
DC10 3E04       00275          LD      A,04H    ;SELECT WR4
DC12 D349       00276          OUT     (49H),A
DC14 3E4C       00277          LD      A,4CH    ;PROGRAM STOP BITS & CLK RATE.
DC16 D349       00278          OUT     (49H),A
DC18 3E05       00279          LD      A,05     ;SELECT WR5
DC1A D349       00280          OUT     (49H),A
DC1C 3E28       00281          LD      A,28H    ;PROGRAM TRANSMIT 7 BITS/CHAR.
DC1E D349       00282          OUT     (49H),A
DC20 3E01       00283          LD      A,01H    ;SELECT WR1
DC22 D349       00284          OUT     (49H),A
DC24 3E00       00285          LD      A,00H    ;NULL IT
                00286
DC26 CD06D0     00287 LOOP     CALL    0D006H   ;GET A CHARACTER.
DC29 D348       00288          OUT     (48H),A  ;SEND CHARACTER,
DC2B CD00DB     00289          CALL    0DB00H   ;DISPLAY PORT MAP.
DC2E 18F6       00290          JR      LOOP
DC30 C9         00291          RET
0000            00292          END
00000 Total errors

LOOP    DC26
```